

WHAT IS CLAIMED IS:

- 1 1. A method comprising:
 - 2 sending bits of data on an input line and on a control
 - 3 line of a test access protocol (TAP) controller of a
 - 4 JTAG-compliant device; and
 - 5 receiving and storing the bits of data from the input
 - 6 line and from the control line at the TAP controller.
- 1 2. The method of Claim 1, wherein the receiving and storing
- 2 are performed in response to the TAP controller being in
- 3 a shift data register state or a pause data register
- 4 state.
- 1 3. The method of Claim 1, wherein the receiving and storing
- 2 are performed in response to a burst-write instruction
- 3 being an active instruction in the TAP controller.
- 1 4. The method of Claim 3, further comprising loading the
- 2 burst-write instruction into an instruction register of
- 3 the TAP controller.
- 1 5. The method of Claim 1, further comprising receiving and
- 2 storing bits in response to:
 - 3 the TAP controller being in an Exit1 data register
 - 4 state, and
 - 5 a burst-write instruction being an active instruction
 - 6 in the TAP controller.
- 1 6. The method of Claim 1, further comprising receiving and
- 2 storing bits in response to:

3 the TAP controller being in an Exit2 data register
4 state, and

5 a burst-write instruction being an active instruction
6 in the TAP controller.

1 7. The method of Claim 1, wherein the storing the bits
2 comprises shifting the bits into a least significant bit
3 of a data register.

1 8. An apparatus comprising:

2 a JTAG-compliant test access protocol (TAP)
3 controller;

4 a control (TMS) line connected to the TAP controller;
5 and

6 an input (TDI) line connected to the TAP controller,
7 the control and input lines adapted to transmit data
8 bits, and

9 the TAP controller adapted to receive and store the
10 data bits transmitted on the control and input
11 lines.

1 9. The apparatus of Claim 8, wherein the TAP controller is
2 adapted to receive the data bits in response to the TAP
3 controller being in a shift data register (Shift-data-
4 register) state or a pause data register (Pause-data-
5 register) state.

1 10. The apparatus of Claim 8, wherein the TAP controller is
2 adapted to receive the data bits in response to a burst-
3 write instruction being an active instruction in the TAP
4 controller.

- 1 11. The apparatus of Claim 8, further comprising a data
2 register accessible by the TAP controller, the data
3 register adapted to store the data bits received from the
4 control line and from the input line.
- 1 12. The apparatus of Claim 11, wherein the data register is
2 adapted to store the data bits by shifting the data bits
3 into a least significant bit of the data register.
- 1 13. The apparatus of Claim 8, wherein the TAP controller is
2 adapted to receive the data bits of in response to:
3 the TAP controller being in an Exit1 data register
4 state, and
5 a burst-write instruction being an active instruction
6 in the TAP controller.
- 1 14. The apparatus of Claim 8, wherein the TAP controller is
2 adapted to receive the data bits of in response to:
3 the TAP controller being in an Exit2 data register
4 state, and
5 a burst-write instruction being an active instruction
6 in the TAP controller.
- 1 15. A computer program product stored on a computer operable
2 media, the computer program product comprising software
3 code effective to:
4 send bits of data on an input line and on a control
5 line of a test access protocol (TAP) controller of a
6 JTAG-compliant device; and

7 receive and store the bits of data from the input line
8 and from the control line at the TAP controller.

1 16. The computer program product of Claim 15, wherein the
2 software code effective to receive and store are each
3 performed in response to the TAP controller being in a
4 shift data register state or a pause data register state.

1 17. The computer program product of Claim 15, wherein the
2 software code effective to receive and store are each
3 performed in response to a burst-write instruction being
4 an active instruction in the TAP controller.

1 18. The computer program product of Claim 17, further
2 comprising software code effective to load the burst-
3 write instruction into an instruction register of the TAP
4 controller.

1 19. The computer program product of Claim 15, further
2 comprising software code effective to receive and store
3 the data bits in response to:

4 the TAP controller being in an Exit1 data register
5 state, and

6 a burst-write instruction being an active instruction
7 in the TAP controller.

1 20. The computer program product of Claim 15, further
2 comprising software code effective to receive and store
3 the data bits in response to:

4 the TAP controller being in an Exit2 data register
5 state, and

6 a burst-write instruction being an active instruction
7 in the TAP controller.

1 21. The computer program product of Claim 15, wherein the
2 software code effective to store the bits comprises
3 software code effective to shift the bits into a least
4 significant bit of a data register.
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